CLAIMS:

1. An electronic device comprising a transistor (100) provided at a surface (11) of a semiconductor substrate (10), the transistor having a source (120) and a drain (220) that are mutually connected through a channel (21), which transistor (100) is further provided with a gate electrode (43) for influencing an electron distribution in the channel (21) and with a shield (50) present between the gate (43) and the drain (220), which drain (220) is provided with a drain extension (25,26) extending in the substrate (10) towards the channel (21), the drain (220) having a contact (41), said drain contact (41) and said gate (43) being mutually separated through an extension area (140), characterized in that the shield (50) has a stepped structure in the extension area (140).

2. An electronic device as claimed in claim 1, wherein a L-shaped spacer (51) is present between the gate-electrode (43) and the shield (50).

3. An electronic device as claimed in claim 1 or 2, wherein the shield (50) is formed as a metal silicide.

4. An electronic device as claimed in claim 1 or 2, wherein the drain extension (25, 26) is provided with a first (25) and a second region (26), the first region (25) having interfaces with the channel (21) and the second region (26), the second region (26) having an interface with a contact area (24) within the drain (220), which first region (25) has a higher dopant concentration than the second region (26), and

wherein the first region (25) is substantially present within a shield area (150) defined by a perpendicular projection of the shield (50) on the substrate (10).

5. An electronic device comprising a transistor (100) provided at a surface (11) of a semiconductor substrate (10), the transistor (100) having a source (120) and a drain (220) that are mutually connected through a channel (21), which transistor (100) is further provided with a gate electrode (43) for influencing an electron distribution in the channel (21) and with a shield (50) present between the gate (43) and the drain (220), which drain (220) is provided

with a drain extension (25,26) extending in the substrate (10) towards the channel (21), the drain (220) having a contact (41), said drain contact (41) and said gate (43) being mutually separated through an extension area (140), which drain extension (25,26) is provided with a first (25) and a second region (26), the first region (25) having interfaces with the channel (21) and the second region (26), the second region (26) having an interface with a contact region (24) within the drain (220),

wherein the first region (25) has a higher dopant concentration than the second region (26), and the first region (25) is substantially present within a shield area (150) defined by a perpendicular projection of the shield (150) on the substrate (10).

6. An electronic device as claimed in claim 4 or 5, wherein the interface between the first and the second region (25,26) is present within the shield area (150).

7. An electronic device as claimed in claim 4, 5 or 6, wherein the ratio of the dopant concentrations in the first and the second region (25,26) is in the range of 1.2 to 2.5.

8. An electronic device as claimed in claim or 5, wherein the shield (50) is electrically connected to the source (120) through an electrical connection.

9. An electronic device as claimed in claim 9, wherein the electrical connection comprises a capacitor.

10. An electronic device as claimed in claim 1 or 5, wherein the semiconductor substrate (10) is made of silicon and the transistor (100) is of the LDMOS type.

11. A method of manufacturing an electronic device as claimed in claim 1, comprising the steps of:

- providing a transistor including source (120), drain (220) and gate (43), said drain (220) being provided with a drain extension (25,26);
- providing insulating material (45,51) on top of and adjacent to the gate (43), and
- providing a stepped shield structure (50) by metal deposition on the insulating material (45,51).